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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,113	09/18/2003	Gabriele Barlocchi	854063.552D1	2816
500 7590 05/29/2007 SEED INTELLECTUAL PROPERTY LAW GROUP PLLC 701 FIFTH AVE SUITE 5400 SEATTLE, WA 98104			EXAMINER ERDEM, FAZLI	
			ART UNIT 2826	PAPER NUMBER
			MAIL DATE 05/29/2007	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	Application No. 10/667,113	Applicant(s) BARLOCCHI ET AL.	
	Examiner Fazli Erdem	Art Unit 2826	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 21 December 2006.
- 2a) ☐ This action is FINAL.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 8-19 and 21-35 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 8-19 and 21-35 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### DETAILED ACTION

US Patent 5,393,375 to MacDonald et al. is included in Form 892. Applicant is directed to Figs. 2F and 4.

#### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 8-13, 19 and 21, rejected under 35 U.S.C. 103(a) as being unpatentable over Sparks et al. (5,719,069) in view of Sparks (5,531,121)

Regarding Claim 8, Sparks et al. disclose a structure formed in a substrate of semiconductor material 10, the structure comprising: at least one trench 10 formed in the substrate, the at least one trench having an open top and an open bottom (Figs 2C, 4a and 6) and a coating 42 in Fig. 6, 7 and 10c, on the lateral walls of the at least one trench with material resistant to etching; a cavity having walls formed below each at least one trench and in communication with the open bottom of the at least one trench, and a coating 42 in Figs 7 and 10c on the walls of the cavity with material inhibiting epitaxial growth; and an silicon layer 36 in Fig. 4b formed on the substrate to cover the open top of the at least one trench and to encase the at least one trench and the cavity in the substrate. Sparks et al. fail to disclose the layer formed on the substrate to cover the cavity to be epitaxial/monocrystalline rather than silicon/polysilicon. However, Sparks discloses a

one-chip integrated sensor process where in Fig. 1, the membrane layer 54 that covers the cavity 22 to be epitaxial.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to replace the polysilicon membrane layer 36 in Sparks et al. with an epitaxial membrane layer as taught by Sparks in order to have a sensor structure with a better compatibility between the substrate/epitaxial layer and the membrane layer since an epitaxial membrane layer would be better compatible with an epitaxial layer.

Regarding Claim 9, Sparks et al. Figs 6, 7 and 10c, disclose a the structure of claim 8, comprising a plurality of trench and cavity pairs 20/22 formed in the substrate

10/14

Regarding Claim 10, in Fig 10c of Sparks et al., each trench and cavity pair 20/22 are formed at different levels within the substrate.

Regarding Claim 11, in Fig 10c of Sparks et al., each trench and cavity pair is formed to have different cross-sectional configurations.

Regarding Claim 12, in Fig 10c of Sparks et al., each trench and cavity pair is formed to have different cross-sectional sizes.

Regarding Claim 13, in Fig. 10c of Sparks et al., each trench and cavity pair 20/22 are formed to have a different cross-sectional size and to be formed at different levels in the substrate 10/14

Regarding Claim 19, in Figs. 4a and 10c Sparks et al. disclose a structure formed in semiconductor material, the structure comprising: a cavity 22 formed in the semiconductor material and having an open top 20; and a membrane 36 in Fig. 46 formed on the semiconductor material that covers the open top of the cavity in the substrate, the membrane having a thickness in the range of between 1 and 3 micrometers.

Sparks et al. fail to disclose the layer formed on the substrate to cover the cavity to be epitaxial/monocrystalline rather than silicon/polysilicon. However, Sparks discloses a one-chip integrated sensor process where in Fig. 1, the membrane layer 54 that covers the cavity 22 to be epitaxial.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to replace the polysilicon membrane layer 36 in Sparks et al. with an epitaxial membrane layer as taught by Sparks in order to have a sensor structure with a better compatibility between the substrate/epitaxial layer and the membrane layer since an epitaxial membrane layer would be better compatible with an epitaxial layer.

Regarding Claim 21, Figs. 4b and 10 of Sparks et al. disclose trenches 20 etched into the membrane 36 and of a depth to be in communication with the cavities 22.

*Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 14-18 and 22-35, rejected under 35 U.S.C. 102(b) as being anticipated by Sparks et al. (5,531,121).

Regarding Claim 14, in Figs. 6 and 10c Sparks et al. disclose a semiconductor material, comprising: a buried cavities 22 formed in the semiconductor material 10/14/56 having an open top 20, the cavity coated with a material 42 inhibiting epitaxial growth; and a membrane 16 formed on the substrate to cover the open top of the cavity to encase the cavity in the substrate.

Regarding Claim 15, wafer of semiconductor material, comprising: a plurality of buried cavities 22 formed in and completely surrounded by the semiconductor material 10/14/56/36, each cavity of the plurality of buried cavities coated with a layer 42 of oxide material inhibiting epitaxial growth.

Regarding Claim 16, the wafer of claim 15, wherein each cavity of the plurality of buried cavities 22 (of two horizontal and one vertical set labeled as 22) are formed parallel to one another and at a right angle with respect to a drawing plane of the semiconductor material.

Regarding Claim 17, the wafer of claim 16, wherein the plurality of cavities are formed at the same height. (horizontal cavities 22 are formed of same height.

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Regarding Claim 18, wafer of claim 16, wherein each of the cavities of the plurality of cavities are formed at a different level (10, 14 and 56) in the semiconductor material.

Regarding Claim 22, in Sparks et al., membrane 36 has a thickness in the range of between 1 and 3 micrometer.

Regarding Claim 23, Figs. 4b and 10 of Sparks et al. disclose trenches 20 etched into the membrane 36 and of a depth to be in communication with the cavities 22.

Regarding Claim 24, element 42 in Fig. 10c of Sparks et al. is TEOS/oxide

Regarding Claim 25, element 42 in Fig. 10c of Sparks et al. is oxide

Regarding Claim 26, elements 50/52 in Fig. 9b-9b of Sparks et al. are nitride materials which could be used to form protective layer around cavity/void 18.

Regarding Claim 27, Fig. 10 of Sparks et al. disclose plurality of buried channels 20a adjacent and separated from each other by dividers 42.

Regarding Claim 28, Fig. 10c of Sparks et al. disclose a wafer of monocrystalline semiconductor material 14/56, comprising at least one buried cavity 22 completely surrounded by said monocrystalline material and covered with a layer of material inhibiting epitaxial growth 42; and a plurality of buried channels 20 adjacent and separated from each other by dividers (dividers are elements 42 in Figs. 6 and 7)

Regarding Claim 29, the wafer of claim 28, wherein the material inhibiting epitaxial growth 42 comprises oxide.

Regarding Claim 30, the wafer of claim 28, wherein the material 42 inhibiting epitaxial growth comprises TEOS/oxide.

Regarding Claim 31, elements 50/52 are in Fig. 9b-9b of Sparks et al. are nitride materials which could be used to form protective layer around cavity/void 18

Regarding Claim 32, in Fig. 10, Sparks et al. disclose a wafer of monocrystalline semiconductor material 14/56, comprising at least one buried cavity 22 completely surrounded by said monocrystalline material and covered with a layer of material inhibiting epitaxial growth 42; and a plurality of buried cavities 22 at different heights within the wafer of monocrystalline semiconductor material.

Regarding Claim 33, the wafer of claim 32, wherein the material inhibiting epitaxial growth 42, comprises oxide.

Regarding Claim 34, the wafer of claim 32, wherein the material inhibiting epitaxial growth 42, comprises TEOS/oxide.

Regarding Claim 35, elements 50/52 are in Fig. 9b-9b of Sparks et al. are nitride materials which could be used to form protective layer around cavity/void 18.

### *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fazli Erdem whose telephone number is (571) 272-1914. The examiner can normally be reached on M - F 8:00 - 5:00.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

FE

May 17, 2007

  
SUE A. PURVIS  
SUPERVISORY PATENT EXAMINER